**Prototype 4 Analysis:**

* Add protection for I/O signals, Add a transient voltage suppressor/ clamping diodes at Isense in order to reduce the reflected noise.
* Probably add two transistors in parallel.
* Change the inductor design. Make it a horizontal mount.
* Find an effective snubbing technique for your high dv/dt node.

Rationalize how to deal with:

* Load Transients
* I/P transients
* Other system variations